Actel
Mask Programmed Gate Arrays

Features

- Mask Programmed versions of Actel Field Programmable Gate Arrays (FPGAs)
- Significant cost reduction for medium- to high-volume applications
- Pin-for-pin compatible with Actel FPGAs
- PCI Local Bus Revision 2 Compliant
- Automatic translation from Actel FPGA netlist to MPGA
- Test vectors generated from customer simulation vectors
- Short lead times for prototype and production devices
- MPGA available for all ACT 1, ACT 2, 1200XL, ACT 3, and 3200DX devices
- Device sizes from 1,200 to 10,000 gates
- Up to 175 user I/Os
- Available in commercial or industrial temperature ranges
- PLCC, PQFP, VQFP, and TQFP packages available
- Meets all internal worst-case FPGA performance specifications
- Lower I/O capacitance than FPGA
- Lower power dissipation than FPGA

Description

The Actel Mask Programmed Gate Array (MPGA) products are masked versions of the popular Actel FPGA families. These semi-custom devices offer the customer a design path that provides significant cost reduction without significant risk or engineering effort. For medium- to high-volume applications in which the design is fixed, the Actel FPGA used for prototyping and initial production can be replaced by the corresponding MPGA device.

Product Family Profile

	Capacity				Available Packages			
MPGA Device Type	**Gate Array Equivalent Gates**	**PLD Equivalent Gates**	**Flip-Flops (Maximum)**	**User I/Os (Maximum)**	**PLCC**	**PQFP**	**VQFP**	**TQFP**
M1010	1,200	3,000	147	57	44, 68-pin	100-pin	80-pin	—
M1020	2,000	6,000	273	69	44, 68, 84-pin	100-pin	80-pin	—
M1225	2,500	6,250	382	83	84-pin	100-pin	100-pin	—
M1240	4,000	10,000	568	104	84-pin	100, 144-pin	—	176-pin
M1280	8,000	20,000	998	140	84-pin	100, 160, 208-pin	—	176-pin
M1415	1,500	3,750	312	80	84-pin	100-pin	100-pin	—
M1425	2,500	6,250	435	100	84-pin	100, 160-pin	100-pin	—
M1440	4,000	10,000	706	140	84-pin	160-pin	100-pin	176-pin
M1460	6,000	15,000	976	167	—	160, 208-pin	—	176-pin
M14100	10,000	25,000	1153	175	—	208-pin	—	—
M3265	6,500	1,600	747	126	84-pin	100, 160-pin		176-pin
M32100	10,000	25,000	1031	152	84-pin	160, 208-pin	—	176-pin
M32140	14,000	35,000	1410	176	84-pin	160, 208-pin	—	176-pin
M32200	20,000	50,000	1822	202	—	208, 240-pin	—	—
M32300	30,000	75,000	2804	250	—	208, 240-pin	—	—
M32400	40,000	100,000	3759	288	—	240-pin	—	—

The granular, regular structure of the Actel antifuse-based FPGA products enables easy conversion to MPGA. Actel provides all required engineering services to convert the customer design from FPGA to MPGA, using proprietary software to automatically convert the FPGA logic design into the MPGA device. Test vector generation is made easy by software that converts the customer's third-party simulation vectors into the final vectors used to test the device in production.

All Actel MPGA devices are pin-for-pin compatible with the corresponding FPGA, and therefore no board redesign is required. MPGA devices meet all worst-case timing specifications of the FPGA devices. MPGA devices are available for all plastic packaged devices from ACT 1, ACT 2, 1200XL, ACT 3, and 3200DX families. See the "Product Plan" on page 1-260 for a detailed list of available device and package combinations.

Actel FPGA to MPGA Design Flow

Actel's three families of FPGA devices offer a wide selection of device sizes, package choices, performance characteristics, and price points. The FPGA families provide the ideal prototyping tool and are cost-effective for low- to medium-volume applications. As volumes increase, a cost-reduction path becomes a key factor to ensure continued success and profitability of the end product. Once the design has stabilized and volumes are increasing, a choice can be made to convert the design to an MPGA. Since the MPGA product is pin-for-pin compatible with the FPGA, no board redesign is required, and the MPGA can directly replace the FPGA.

A typical design process uses the FPGA device as the prototyping and initial production product of choice and converts to the MPGA as volumes warrant. Figure 1 shows the design process for Actel FPGA and MPGA devices. This option gives you the flexibility to adjust volumes as the demand for the end product changes. Since the MPGA is a semicustom device, all production is built to your order. If the design is already completed in the FPGA, any demand upsides can be satisfied by temporarily switching production back to the FPGA. Since Actel FPGAs are standard off-the-shelf devices, additional product requirements can be met within a short lead time.

The Actel FPGA devices offer the easiest and fastest way to bring a new product to market, and the three FPGA families offer a wide selection of low-cost, high-performance devices. The addition of the MPGA devices offers a simple, low-risk cost-reduction path as production volumes increase.

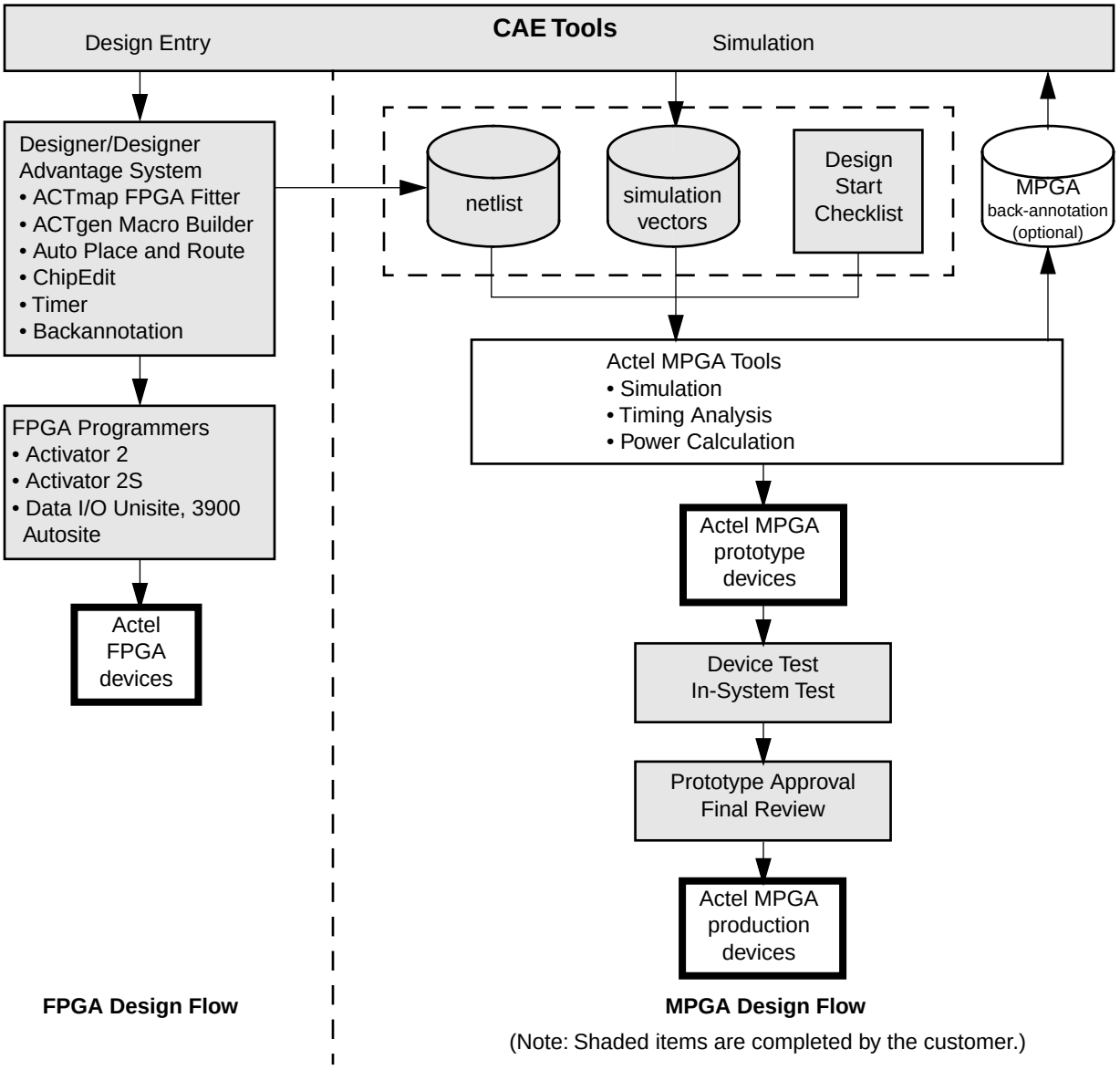


Figure 1 • *Actel Device Design Flow*

Product Plan

	Availability	Application	
ACT 1 Family		**Commercial**	**Industrial**
M1010 Device			
44-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔
68-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔
80-pin Very Thin Plastic Quad Flatpack (VQFP)	✔	✔	—
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
M1020 Device			
44-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔
68-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔
80-pin Very Thin Plastic Quad Flatpack (VQFP)	✔	✔	—
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
ACT 2/1200XL Family			
M1225 Device			
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
100-pin Thin Plastic Quad Flatpack (TQFP)	✔	✔	—
M1240 Device			
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
144-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
176-pin Thin Plastic Quad Flatpack (TQFP)	✔	✔	—
M1280 Device			
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
176-pin Thin Plastic Quad Flatpack (TQFP)	✔	✔	—
ACT 3 Family			
M1415 Device			
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
100-pin Very Thin Plastic Quad Flatpack (VQFP)	✔	✔	—
Note:*M1425 Device*			
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
100-pin Very Thin Plastic Quad Flatpack (VQFP)	✔	✔	—
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
M1440 Device			
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔
100-pin Very Thin Plastic Quad Flatpack (VQFP)	✔	✔	—
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
176-pin Thin Plastic Quad Flatpack (TQFP)	✔	✔	—
M1460 Device			
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
176-pin Thin Plastic Quad Flatpack (TQFP)	✔	✔	—
208-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
M14100 Device			
208-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔

Product Plan (continued)

	Availability	Application	
3200DX Family			
M3265 Device			
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
176-pin Thin Plastic Quad Flatpack (TQFP)	✔	✔	✔
M32100 Device			
84-pin Plastic Leaded Chip Carrier (PLCC)	P	P	P
160-pin Plastic Quad Flatpack (PQFP)	P	P	P
208-pin Plastic Quad Flatpack (PQFP)	P	P	P
176-pin Thin Plastic Quad Flatpack (TQFP)	P	P	P
M32140 Device			
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
208-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
176-pin Thin Plastic Quad Flatpack (TQFP)	✔	✔	✔
M32200 Device			
208-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
240-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
176-pin This Plastic Quad Flatpack (TQFP)	✔	✔	✔
M32300 Device			
208-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔
240-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔

Availability: ✔ = Available
P = Planned
— = Not Planned

ACT 1 Device Resources

MPGA Device Type	Gate Array Equivalent Gates	User I/Os				
		PLCC			PQFP	VQFP
		44-pin	68-pin	84-pin	100-pin	80-pin
M1010	1200	34	57	57	57	57
M1020	2000	34	57	69	69	69

ACT 2/1200XL Device Resources

MPGA Device Type	Gate Array Equivalent Gates	User I/Os						
		PLCC	PQFP				VQFP	TQFP
		84-pin	100-pin	144-pin	160-pin	208-pin	100-pin	176-pin
M1225	2500	72	83	—	—	—	83	—
M1240	4000	72	83	104	—	—	—	104
M1280	8000	72	83	—	125	140	—	140

ACT 3 Device Resources

MPGA Device Type	Gate Array Equivalent Gates	User I/Os					
		PLCC	PQFP			VQFP	TQFP
		84-pin	100-pin	160-pin	208-pin	100-pin	176-pin
M1415	1500	70	80	—	—	80	—
M1425	2500	70	80	100	—	83	—
M1440	4000	70	—	131	—	83	140
M1460	6000	—	—	131	167	—	151
M14100	10000	—	—	—	175	—	—

3200DX Device Resources

MPGA Device Type	Gate Array Equivalent Gates	User I/Os					
		PLCC	PQFP				TQFP
		84-pin	100-pin	160-pin	208-pin	240-pin	176-pin
M3265	6500	72	83	125	—	—	126
M32100	10000	72	—	125	156	—	151
M32140	14000	72	—	125	176	—	151
M32200	20000	—	—	—	176	TBD	—
M32300	30000	—	—	—	176	TBD	—
M32400	40000	—	—	—	—	TBD	—

Ordering Information

M14100 – **RQ** **208** **C**

Application (Temperature Range)
C = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)

Package Lead Count

Package Type
PL = Plastic Leaded Chip Carrier (PLCC)
PQ = Plastic Quad Flatpack (PQFP)
TQ = Thin (1.4 mm) Plastic Quad Flatpack (TQFP)
VQ = Very Thin (1.0 mm) Plastic Quad Flatpack (VQFP)
RQ = Power Plastic Quad Flatpack (RQFP)

Part Number
M1010= 1200 Gates—ACT 1
M1020= 2000 Gates—ACT 1
M1225= 2500 Gates—ACT 2/1200XL
M1240= 4000 Gates—ACT 2/1200XL
M1280= 8000 Gates—ACT 2/1200XL
M1415= 1500 Gates—ACT 3
M1425= 2500 Gates—ACT 3
M1440= 4000 Gates—ACT 3
M1460= 6000 Gates—ACT 3
M14100=10000 Gates—ACT 3
M3265= 6500 Gates—3200DX
M32100=10000 Gates—3200DX
M32140=14000 Gates—3200DX
M32200=20000 Gates—3200DX
M32300=30000 Gates—3200DX
M32400=40000 Gates—3200DX

Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	–0.3 to +7.0	V
V_I	Input Voltage	–0.3 to V_{CC} +0.3	V
V_O	Output Voltage	–0.3 to V_{CC} +0.3	V
I_{IO}	I/O Source Sink Current	±20	mA
T_{STG}	Storage Temperature	–55 to +125	°C

Note:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range	0 to +70	–40 to +85	°C
Power Supply Tolerance	±5	±10	%V_{CC}

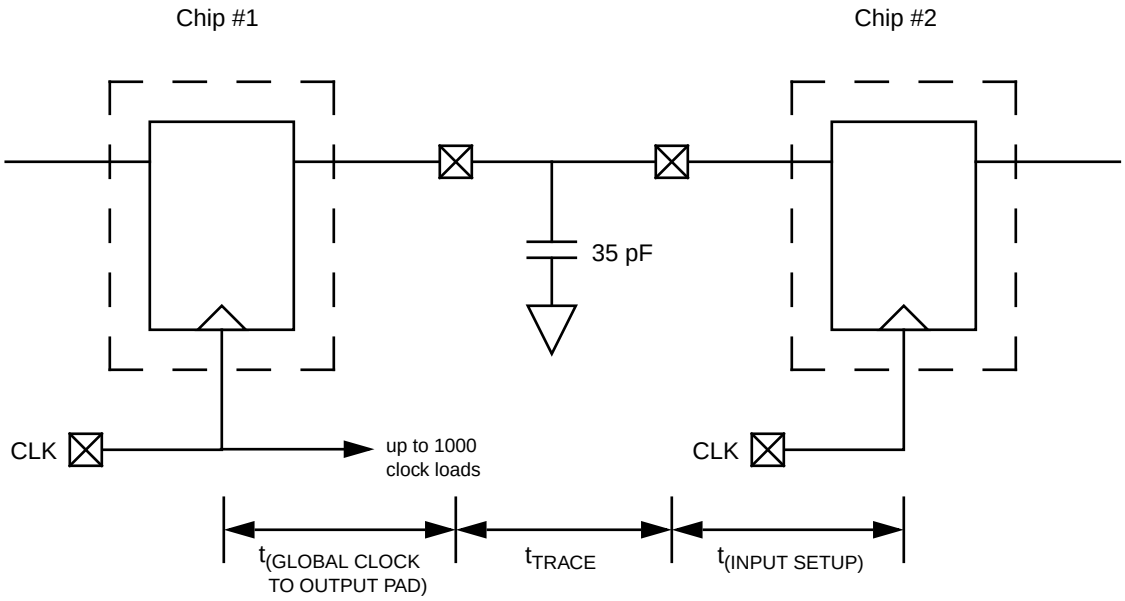
Electrical Specifications

Symbol	Parameter	Test Condition	Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V_{OH}[1,2]	HIGH Level Output	I_{OH} = –6 mA (CMOS)	3.7		3.7		V
		I_{OH} = –8 mA (TTL)[3]	2.4		2.4		V
V_{OL}[1,2]	LOW Level Output	I_{OL} = +6 mA (CMOS)		0.4		0.4	V
		I_{OL} = +8 mA (TTL)[3]		0.4		0.4	V
V_{IH}	HIGH Level Input	TTL Inputs	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	LOW Level Input	TTL Inputs	–0.3	0.8	–0.3	0.8	V
I_{IN}	Input Leakage	V_I = V_{CC} or GND	–1	+1	–1	+1	µA
I_{OZ}	3-state Output Leakage	V_O = V_{CC} or GND	–10	+10	–10	+10	µA
C_{IO}	I/O Capacitance[3]			10		10	pF
$I_{CC(S)}$	Standby Supply Current	V_I = V_{CC} or GND, I_O = 0 mA		100		500	µA

Notes:

1. *Actel devices can drive and receive either CMOS or TTL signal levels. No assignment of I/Os as TTL or CMOS is required.*
2. *Tested one output at a time, V_{CC} = min.*
3. *Not tested, for information only.*

Chip-to-Chip Performance



Chip-to-Chip Performance (Worst-Case Commercial)					
	$t_{(GLOBAL\ CLOCK\ TO\ OUPUT\ PAD)}$	t_{TRACE}	$t_{(INPUT\ SETUP)}$	Total	MHz
Actel MPGA	12.7	1.0	3.1	16.8	60

Pin Description

Package pin assignments for an FPGA design are directly transferred to the equivalent MPGA package because all I/O and power pins are located in identical positions. While the conversion of package pin assignments is transparent in the end product, there are two small functional differences to note between the device types. First, dedicated FPGA global and debugging pins are general purpose MPGA I/O pins. Also, dedicated FPGA programming voltage pins are Vcc or ground pins on an MPGA. Refer to Table 1 for a complete cross-reference of pin descriptions between the FPGA and MPGA.

Table 1 • *FPGA-to-MPGA Pin Cross-Reference*

FPGA Pin Description		MPGA Pin Description
CLK Clock (ACT 1 only) TTL Clock input for ACT 1 global clock distribution network. This pin can also be used as an I/O.	→	**No Change** If desired, TTL Clock input signals may be moved to any MPGA I/O location.
CLKA Clock A (ACT 3, 3200DX, 1200XL, and ACT 2 only) TTL Clock input for clock distribution networks. This pin can also be used as an I/O.	→	**No Change** If desired, TTL Clock input signals may be moved to any MPGA I/O location.
CLKB Clock B (ACT 3, 3200DX, 1200XL, and ACT 2 only) TTL Clock input for clock distribution networks. This pin can also be used as an I/O.	→	**No Change** If desired, TTL Clock input signals may be moved to any MPGA I/O location.
DCLK Diagnostic Clock TTL Clock input for diagnostic probe and device programming. Function is controlled by the MODE pin.	→	**I/O** This pin is used as an I/O only. It is not used for diagnostic probe or device programming functions on an MPGA.
GND Ground LOW supply voltage.	→	**Ground** LOW supply voltage.
HCLK Dedicated (Hard-wired) Array Clock (ACT 3 only) TTL Clock input for ACT 3 sequential modules. This pin can also be used as an I/O.	→	**No Change** If desired, TTL Clock input signals may be moved to any MPGA I/O location.
I/O Input/Output The I/O pin functions as an input, output, three-state, or bidirectional buffer. Unused pins are automatically driven LOW by the Designer software.	→	**I/O** User-defined MPGA I/O pins function identically to their FPGA counterparts. However, unused pins are NC (no connection) pins.
IOCLK Dedicated (Hard-wired) I/O Clock (ACT 3 only) TTL Clock input for ACT 3 I/O modules. This pin can also be used as an I/O.	→	**No Change** If desired, TTL Clock input signals may be moved to any MPGA I/O location.
IOPCL Dedicated (Hard-wired) I/O Preset/Clear (ACT 3 only) TTL input for ACT 3 I/O preset or clear. This pin can also be used as an I/O.	→	**No Change** If desired, this input signal may be moved to any MPGA I/O location.
MODE Mode The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os.	→	**TEST (No Connection)** This pin is reserved for parametric testing and should be connected to ground (LOW supply voltage).

Table 1 • *FPGA-to-MPGA Pin Cross-Reference (continued)*

FPGA Pin Description		MPGA Pin Description
NC No Connection This pin is not connected to circuitry within the device.	→	**NC No Connection** This pin is not connected to circuitry within the device.
PRA Probe A The Probe A pin is used for FPGA diagnostics. Function is controlled by the MODE pin.	→	**I/O** This pin is used as an I/O only. It is not used for diagnostic probe or device programming functions on an MPGA.
PRB Probe B The Probe B pin is used for FPGA diagnostics. Function is controlled by the MODE pin.	→	**I/O** This pin is used as an I/O only. It is not used for diagnostic probe or device programming functions on an MPGA.
QCLKA/B,C,D Quadrant Clock (Input/Output) (3200DX only) These four pins are the quadrant clock inputs. When not used as a register control signal, these pins can function as general purpose I/O.	→	**No Change** If desired, TTL Clock input signals may be moved to any MPGA location.
SDI Serial Data Input Serial data input for diagnostic probe and device programming. Function is controlled by the MODE pin.	→	**I/O** This pin is used as an I/O only. It is not used for diagnostic probe or device programming functions on an MPGA.
TCK Test Clock (3200DX only) Clock signal to shift the JTAG data into the device. This pin functions as an I/O when the JTAG fuse is not programmed	→	**No Change**
TDI Test Data In (3200DX only) Serial data input or JTAG instructions and data. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed.	→	**No Change**
TDO Test Data Out (3200DX only) Serial data output for JTAG instructions and test data. This pin functions as an I/O when the JTAG fuse is not programmed.	→	**No Change**
TMS Test Mode Select (3200DX only) Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed.	→	**No Change**
V_{CC} Supply Voltage HIGH supply voltage.	→	**V_{CC}** HIGH supply voltage.

MPGA Architecture

The Actel MPGA is built using a "sea-of-gates" architecture. A solid, regularly ordered array of transistors is overlaid with a multilevel metal interconnect. Surrounding this logic core is an array of programmable power and I/O pads. Separate grids provide power and ground supplies for the core logic and I/O cells.

The highly dense structure of Actel MPGAs provides for a cost-effective solution while maintaining the high performance of each particular design. This architecture reduces die size for low cost while minimizing gate length and shortening routing paths for excellent system performance. The robust power supply grids provide high I/O current drive without sacrificing high noise immunity. Since Actel FPGAs use a similar gate array architecture, design migration is a straightforward, simple process. Because of the advanced technology employed by the MPGA, the internal and external performance of each design is virtually assured to be preserved or improved after migration. To simplify migration further, the I/O pads are carefully arranged to allow FPGA pin assignments to be directly transferred to the full line of MPGA packages. For more information about the ease of design migration from Actel FPGAs to MPGAs, see the application note "Designing for Migration to Actel MPGAs."

Power Dissipation

The power dissipation for an Actel MPGA is composed of two parts: static power and active power. The static power is a product of the standby supply current (Icc) and the DC supply voltage (Vcc). Specifications for Icc and Vcc are located in the "Electrical Specifications" section of this data sheet. The active power is a product of equivalent capacitance, square of the DC supply voltage, and average switching frequency of the circuit. It is expressed in the formula

$$\text{Power } (\mu W) = C_{EQ} \bullet V_{CC}^2 \bullet f$$

where

C_{EQ} is the equivalent capacitance in picofarads (pF)

V_{CC} is the DC supply voltage in volts (V)

f is the switching frequency in megahertz (MHz)

Upon receipt of the "Design Start Checklist" and associated materials, Actel calculates the MPGA active power dissipation for each design based on this formula. This calculation is immediately relayed to you so that you can update system power specifications accordingly. Typically, power dissipation of an Actel design is significantly lower for the MPGA version versus the FPGA version.

Timing Characteristics

The timing characteristics for Actel MPGA devices are consistent across family and device types. Typical I/O buffer, internal logic cell, and internal routing delays are common to all MPGA devices. The advanced technology of the devices ensures converted designs meet or exceed FPGA performance. Refer to the MPGA Timing Model diagram and Timing Characteristics chart for detailed timing and delay estimates.

Timing Derating

Timing derating factors due to temperature, voltage, and process variations are summarized in the following tables and graphs. Use these derating factors to determine device performance at any particular condition within the electrical and environmental specifications.

MPGA devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

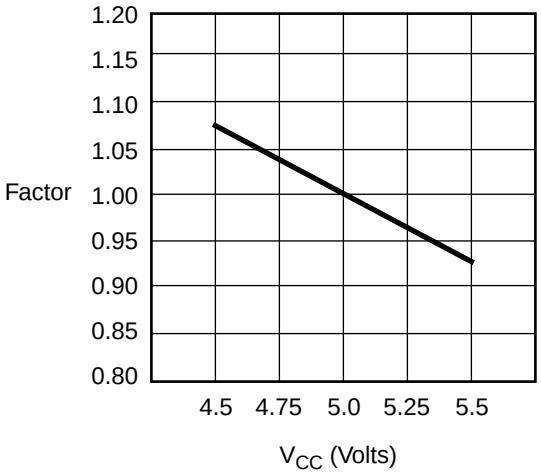
Timing Derating Factor, Temperature and Voltage

	Industrial	
	Minimum	Maximum
(Commercial Minimum/Maximum Specification) x	0.85	1.07

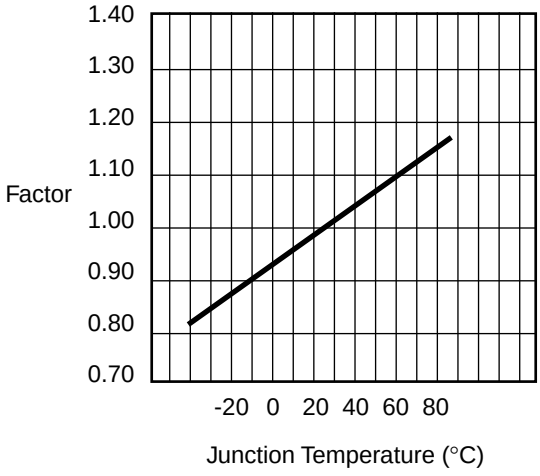
Timing Derating Factor for Designs at Typical Temperature (T_J = 25°C) and Voltage (V_{CC} = 5.0 V)

(Commercial Maximum Specification) x	0.86

Voltage Derating Curve

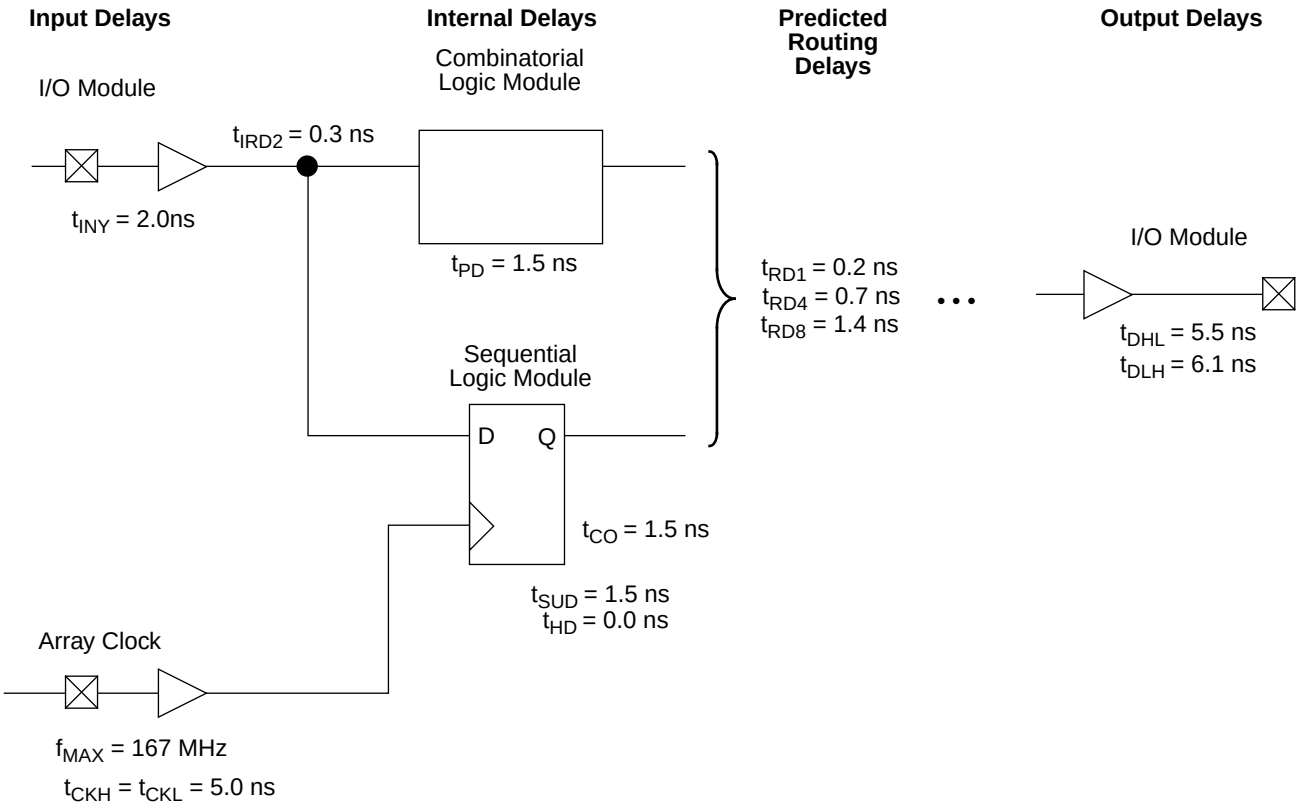


Temperature Derating Curve

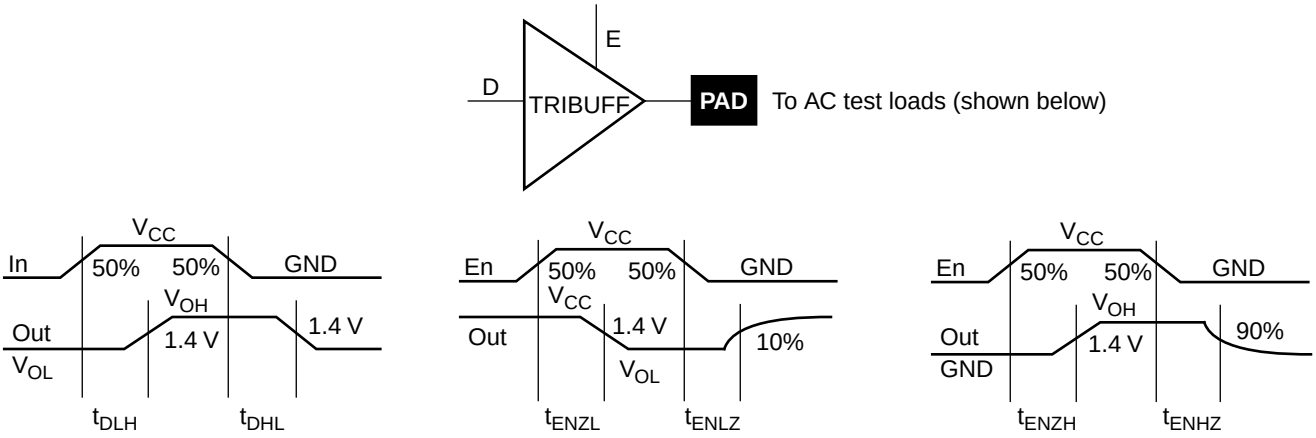


Note: *This derating factor applies to all routing and propagation delays.*

MPGA Timing Model

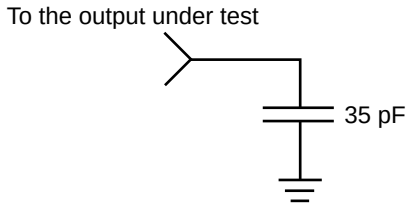


Output Buffer Delays

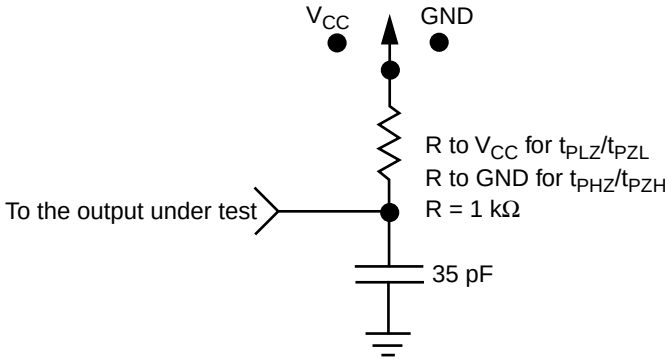


AC Test Loads

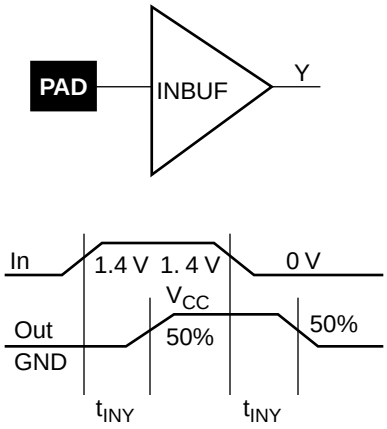
Load 1
(Used to measure propagation delay)



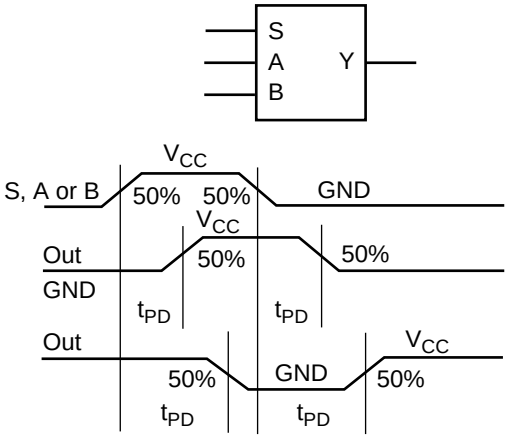
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

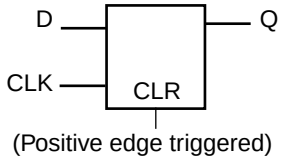


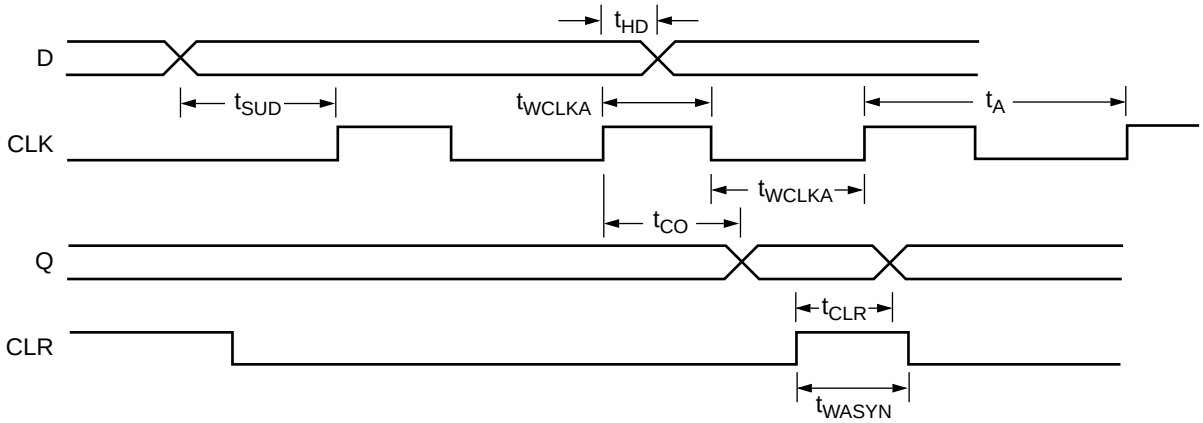
Module Delays



Sequential Module Timing Characteristics

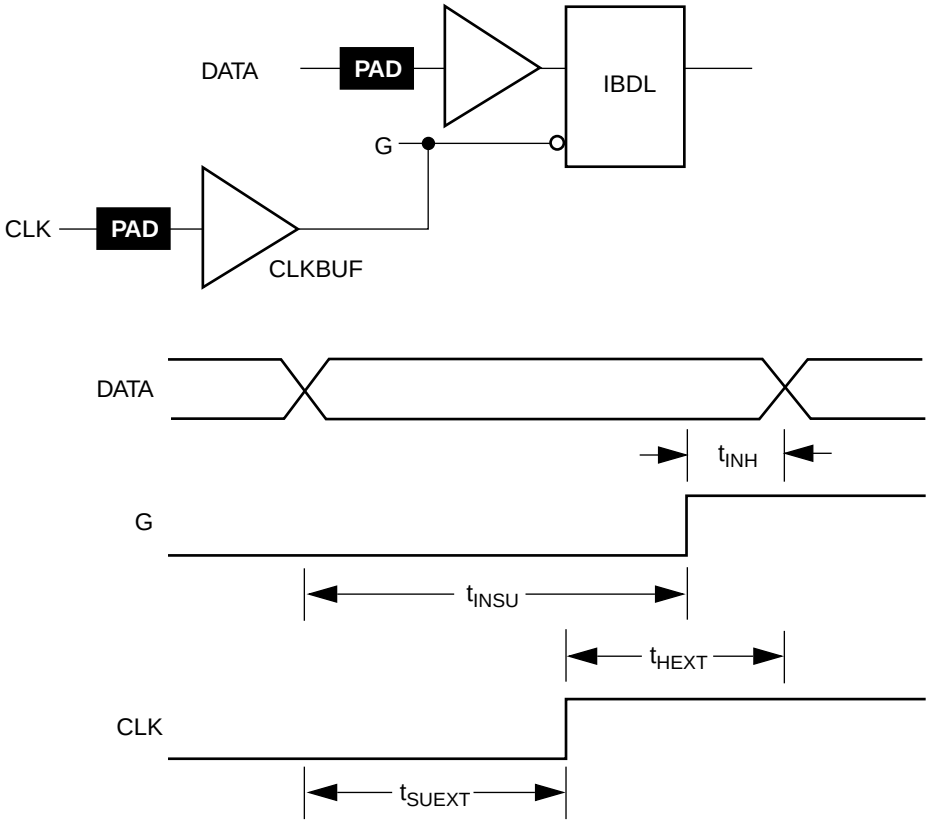
Flip-Flops



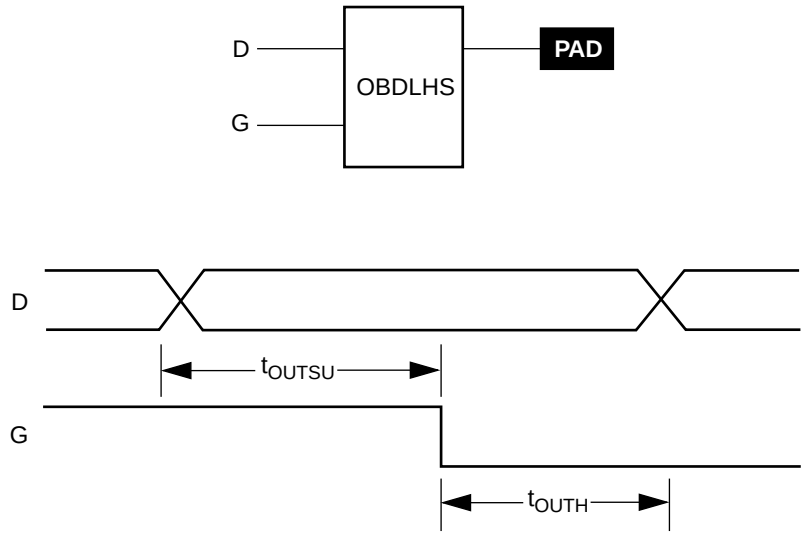


Sequential Timing Characteristics (continued)

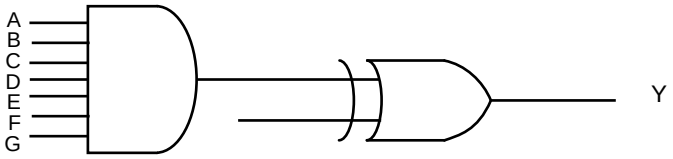
Input Buffer Latches (3200DX only)

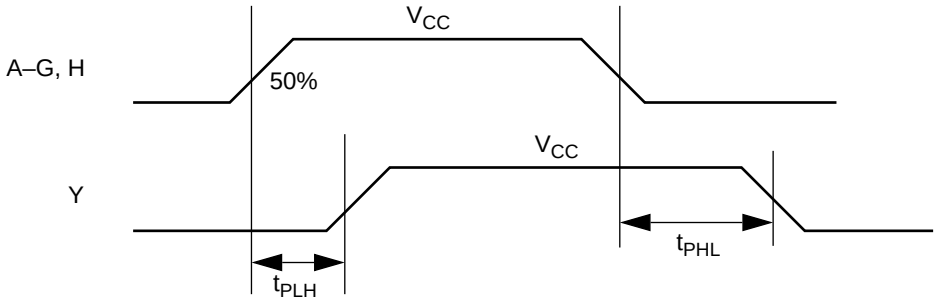


Output Buffer Latches (3200DX only)

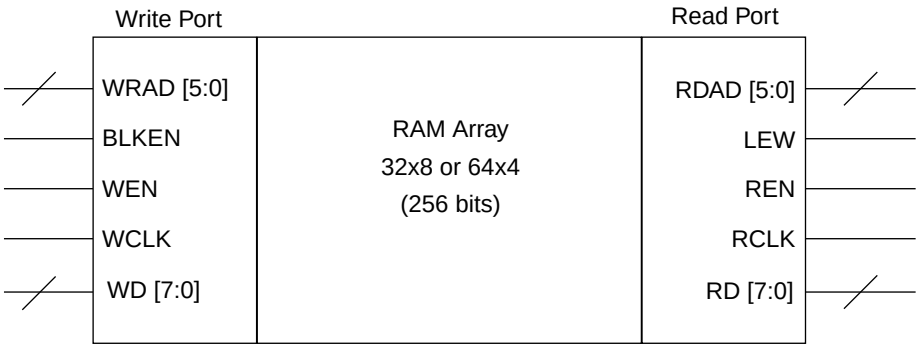


Decode Module Timing (3200DX only)



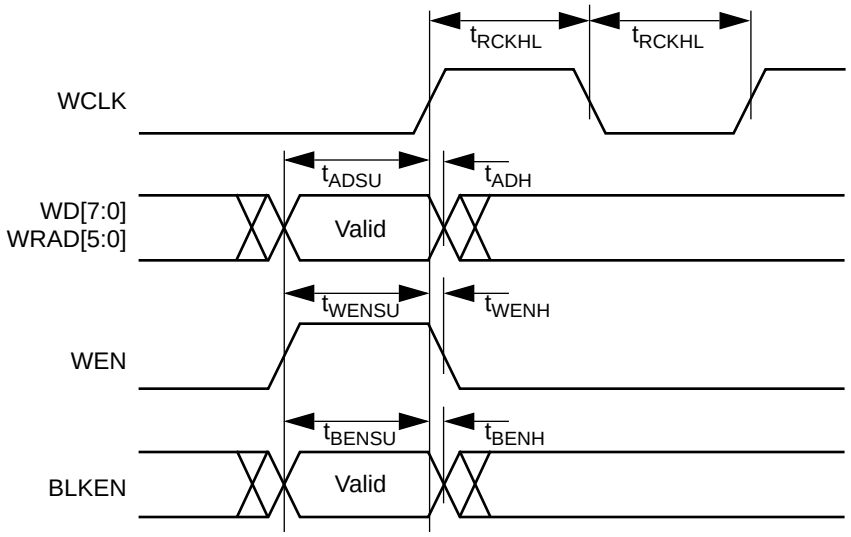


SRAM Timing Characteristic (3200DX only)



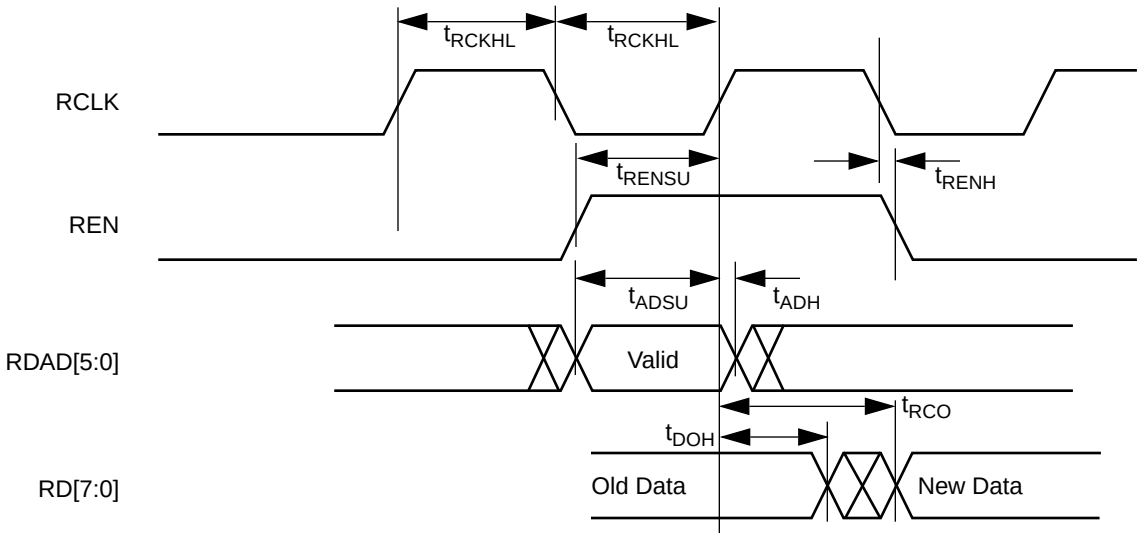
Dual-Port SRAM Timing Waveforms

SRAM Write Operation (3200DX only)



Note: *Identical timing for falling-edge clock.*

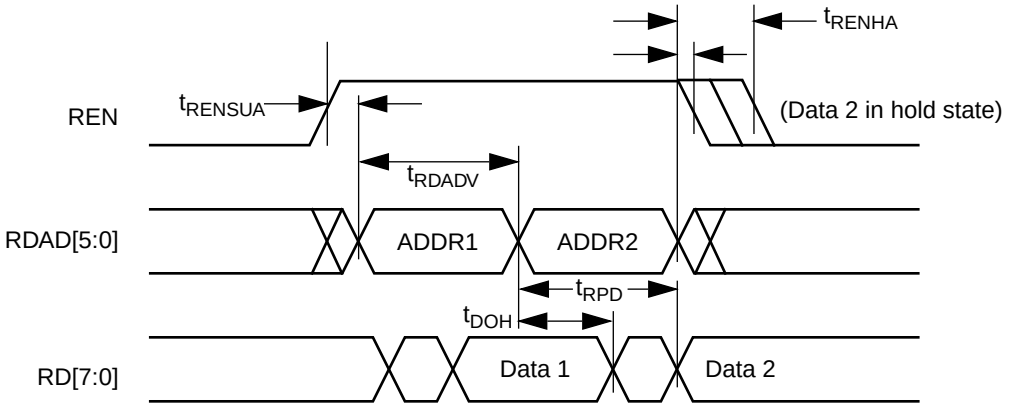
SRAM Synchronous Read Operation (3200DX only)



Note: *Identical timing for falling-edge clock*

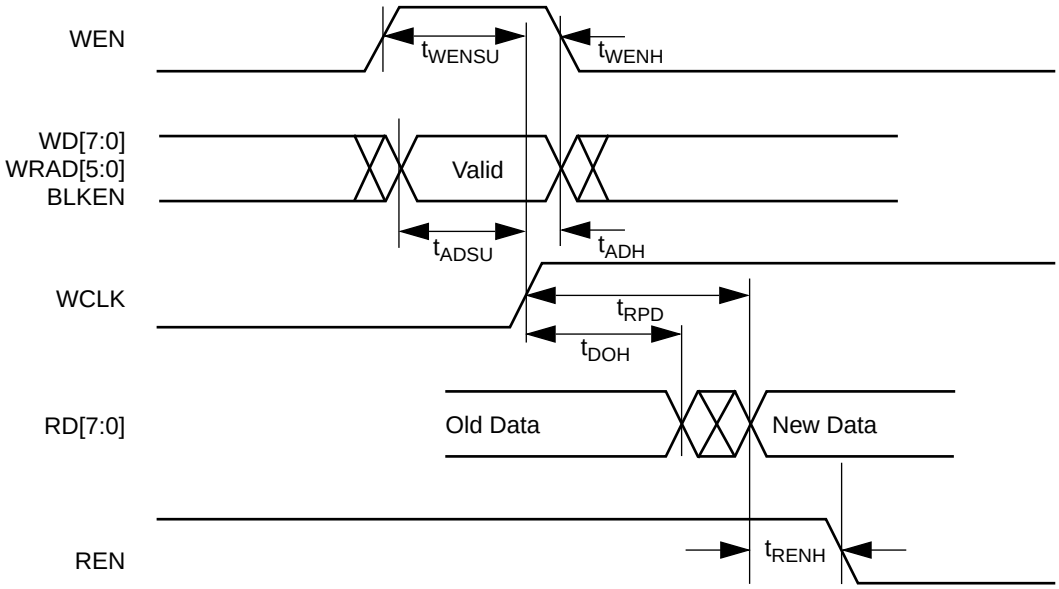
SRAM Asynchronous Read Operation—Type 1 (3200DX only)

((Read Address Controlled)



SRAM Asynchronous Read Operation—Type 2 (3200DX only)

(Write Address Controlled)



MPGA Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

		Preliminary Information		
Logic Module Propagation Delays				
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		1.5	ns
t_{CO}	Sequential Clock to Q		1.5	ns
t_{CLR}	Asynchronous Clear to Q		1.5	ns
Predicted Routing Delays[1]				
t_{RD1}	FO=1 Routing Delay		0.2	ns
t_{RD2}	FO=2 Routing Delay		0.3	ns
t_{RD3}	FO=3 Routing Delay		0.5	ns
t_{RD4}	FO=4 Routing Delay		0.7	ns
t_{RD8}	FO=8 Routing Delay		1.4	ns
Logic Module Sequential Timing				
t_{SUD}	Flip-Flop Data Input Setup	1.5		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		ns
t_{SUD}	Latch Data Input Setup	1.5		ns
t_{HD}	Latch Data Input Hold	0.0		ns
t_{WASYN}	Asynchronous Pulse Width	2.0		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	2.0		ns
t_A	Flip-Flop Clock Input Period	8.0		ns
f_{MAX}	Flip-Flop Clock Frequency		125	MHz
I/O Module Input Propagation Delay				
t_{INY}	Input Data Pad to Y		2.0	ns
Predicted Input Routing Delays[1]				
t_{IRD1}	FO=1 Routing Delay		0.2	ns
t_{IRD2}	FO=2 Routing Delay		0.3	ns
t_{IRD3}	FO=3 Routing Delay		0.5	ns
t_{IRD4}	FO=4 Routing Delay		0.7	ns
t_{IRD8}	FO=8 Routing Delay		1.4	ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Postroute timing analysis or simulation is required to determine actual worst-case performance. Postroute timing is based on actual routing delay measurements performed on the device prior to shipment.*

MPGA Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		
I/O Module – TTL Output Timing[1]				
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{DHL}	Data to Pad, High to Low		6.8	ns
t_{DLH}	Data to Pad, Low to High		3.9	ns
t_{ENZH}	Enable to Pad, Z to High		4.5	ns
t_{ENZL}	Enable to Pad, Z to Low		6.8	ns
t_{ENHZ}	Enable to Pad, High to Z		3.8	ns
t_{ENLZ}	Enable to Pad, Low to Z		2.0	ns
d_{TLH}	Delta Low to High		0.05	ns/pF
d_{THL}	Delta High to Low		0.09	ns/pF
I/O Module – CMOS Output Timing[1]				
t_{DHL}	Data to Pad, High to Low		5.5	ns
t_{DLH}	Data to Pad, Low to High		6.1	ns
t_{ENZH}	Enable to Pad, Z to High		6.7	ns
t_{ENZL}	Enable to Pad, Z to Low		5.6	ns
t_{ENHZ}	Enable to Pad, High to Z		3.8	ns
t_{ENLZ}	Enable to Pad, Low to Z		2.0	ns
d_{TLH}	Delta Low to High		0.09	ns/pF
d_{THL}	Delta High to Low		0.07	ns/pF
Global Clock Networks (for Fanout = 1000)				
t_{CKH}	Input Low to High		5.0	ns
t_{CKL}	Input High to Low		5.0	ns
t_{PWH}	Min. Pulse Width High	2.9		ns
t_{PWL}	Min. Pulse Width Low	2.9		ns
t_{CKSW}	Maximum Skew		0.4	ns
t_P	Minimum Period	6.0		ns
f_{MAX}	Maximum Frequency		167	MHz

Note:

1. Delays based on 35pF loading.